Laboratory 3

(Due date: **004/011**: Oct. 12th, **005**: Oct. 13th, **007**: Oct. 14th)

Objectives

- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

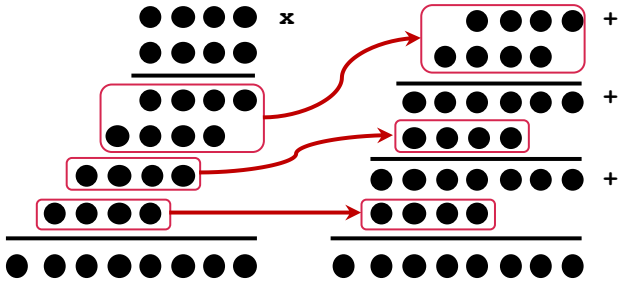
VHDL Coding

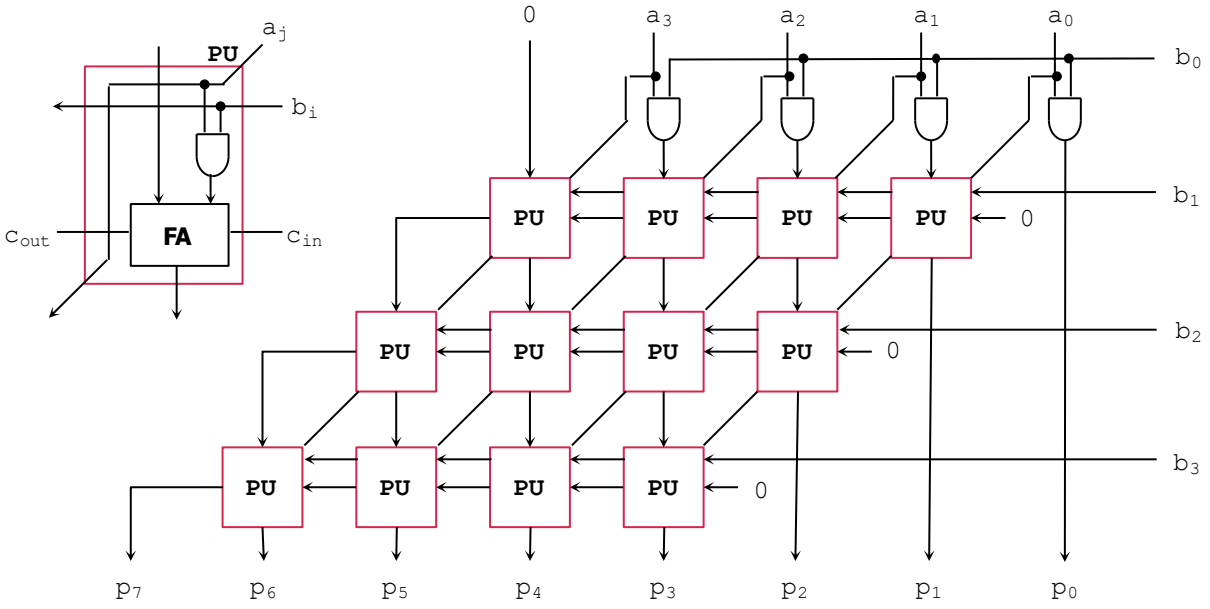
- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

First Activity (100/100)

Design Problem

- The figure depicts an array multiplier for two 4-bit unsigned numbers. It is a straightforward implementation based on adding two partial products (rows) at each stage.





Procedure

- **Vivado: Complete the following steps**:
  - ✓ Create a new Vivado Project. Select the corresponding Artix-7 FPGA device (e.g.: the XC7A50T-1CSG324 FPGA device for the Nexys A7-50T).
  - ✓ Write the VHDL code for this unsigned array multiplier. Synthesize your code.
    - Use the Structural Description: Create a separate `.vhd` file for the Full Adder, the Processing Unit (PU), and the top file (Array Multiplier).
  - ✓ Write the VHDL testbench to test the circuit for all possible cases (256 cases). Use '*for loop*'.
  - ✓ Perform Functional Simulation and Timing Simulation of your design. **Demonstrate this to your TA**.
    - Your simulation might need more time than Vivado Simulator's default (1 us). For example, to add 5 us, you can go to the TCL console and type: `run 5 us` ↵
    - Note that you can represent your data as unsigned integers (use Radix → Unsigned Decimal).

Instructor: Daniel Llamocca
TAs: Sumati Gupta, Fizza Shamim, Moath Algharibeh

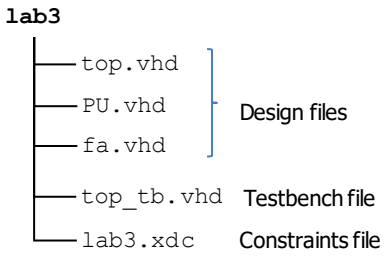
- ✓ I/O Assignment: Generate the XDC file associated with your board.
  - Suggestion:

Board pin names	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
Signal names in code	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

  - The board pin names are used by all the listed boards (Nexys A7-50T/A7-100T, Basys 3, Nexys 4/DDR). The I/Os listed here are all active high.

- ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA**.

- Submit (as a .zip file) the five generated files: VHDL code (3 files), VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.
  - ✓ Your .zip file should only include one folder. Do not include subdirectories.
    - It is strongly recommended that all your design files, testbench, and constraints file be located in a single directory. This will allow for a smooth experience with Vivado.



TA signature: _____ **Date:** _____